Digital System Design (CSC-359)
Tribhuvan University
Institute of Science and Technology
Soch College of Information Technology
Bachelor of Science in Computer Science and Information Technology

Course Title: Digital System Design
Course no: CSC-359 ---------- **Full Marks:** 60+20+20
Credit hours: 3 ---------- **Pass Marks:** 24+8+8
Nature of course: Theory (3 Hrs.) + Lab (3 Hrs.)
Course Synopsis: This course introduces the concepts of VLSI design and testing
Goal: The course objective is to provide ample knowledge on digital design process with the VLSI design procedures and to enhance the knowledge of hardware design applying subsystem design with VHDL and FPGA.

Course Contents:

Unit 1. Introduction ---------- 5 Hrs.
Digital Systems and Integration, Electronic Design Automation, IC Manufacturing, Logic Families, IC Design Techniques, IC characteristics: fan-out, power dissipation, propagation delay, and noise margin of TTL and CMOS integrated circuit logic devices

Unit 2. Logic Manipulation ---------- 5 Hrs.
DeMorgan's Theorem, Canonical Forms, Minterm and Maxterm, implicant, prime implicant, K-Maps, Quine-McCluskey Method.

Unit 3. Application Specific Devices---------- 8 Hrs.
PROMs and EPROMs, Programmable Array Logic (PAL), Programmed Logic Array (PLA), Gate Arrays, Programmable Gate Array, Full Custom Design.

Unit 4. State Machine and Design ---------- 7 Hrs.
Mealy and Moore machines, state transition tables and diagrams, algorithmic state machine charts, Synchronous State Machine Design, Design of Input Forming Logic and Output Forming Logic of state machine.

Unit 4. VLSI Design ---------- 8 Hrs.
Transistor and Layouts, Fabrication Process, Design Rules, Layout design and tools, Logic Gates, Combinational logic Networks and Design, Sequential Systems and Design, Subsystem Design, Various Floorplanning Methods, Off-Chip Connections.

Unit 5. Testing ---------- 6 Hrs.
Testing and Verification, Testing logic circuits, Combinational gate testing, Combinational network testing, Sequential Testing, Test vector generation, fault, fault model and fault detection,

SA0, SA1, Design for Testability.

Unit 6. Hardware Description Languages ---------- 6 Hrs.
VHDL and its use in programmable logic devices (PLDs) like FPGA

Text / Reference Book:
Wolf, Wayne, Modern VLSI Design-Systems on Silicon , Third Edition, Pearson
Comer, David J. Digital Logic State Machine Design, Third Edition, Oxford University Press
Ashenden, Peter J., The Student's Guide to VHDL, Morgan Kaufman